INDUSTRIAL MICRO SYSTEMS

MODEL 282 16K BYTE STATIC RAM MEMORY BOARD

The 282 board is fully STATIC and fully BUFFERED and uses 2114 type memory I.C.'s. The boards are supplied fully tested and burned-in at 70° under diagnostic test to insure reliable operations.

FEATURES

1. Memory Management. On board memory management system.

2. ROM Compatibility. Logic provided to de-activate a portion of memory if ROM is used. A "Phantom Line" is also provided for systems using this feature.

3. Front Panel Independent. Logic provided for compatibility with or without front panels. No front panel modifications are required.

OPTION SELECTION

All option jacks are clearly labeled. With the connector edge of the board toward the viewer, the jacks are located on the right edge and bottom edge of the board. Options are selected by placing shunts (provided) on the jacks. Spare shunts may be left on the board for future use in the event that changes are made in the selected options.

MEMORY ADDRESS SELECTION

A single shunt must be placed on the memory address (MEM ADD) jack located at the top right corner of the board. Four positions, labeled 0, 1, 2, 3, correspond to the four possible address ranges for the 16K block of memory.

Shunt Position	Memory Addresses (HEX)
0	0000 – 3FFF
1	4000 – 7FFF
2	8000 – BFFF
3	C000 – FFFF

FRONT PANEL OPTION

A single shunt must be placed on the front panel option jack (J2) located to the left of the memory address jack. Two positions are possible, the PWR

FRONT PANEL OPTION (Continued)

position for use with systems not having front panels and the MWR position for systems with front panels. When in the PWR positions, the memory write strobe is derived from the 'Processor Write" signal (Pin 77 on the Bus) . When in the MWR position, the "Memory Write" signal (Pin 68 on the Bus) is used to generate a write strobe.
Caution. On some systems not having front panels, the processor board generates a 'Memory Write" signal and in this case, the MWR position should be used. e.g. (Alpha-Micro).

ROM COMPATIBILITY OPTIONS

On systems using ROM's, the RAM memory with corresponding addressing must be deselected when operating in ROM. Two systems are currently popular -

A. "Bootstrap" ROM's used to initially load the memory and not used thereafter.

B. "Dedicated" ROM's which permanently use some portion of the addressable 64K,

Some "Bootstrap" ROM's have been implemented using a "Phantom Line" (Fin 67 on the Bus). When the ROM is active, the "Phantom Line" is held low by the ROM and provides a signal which is used to deselect RAM memory.

"Dedicated" ROM's could, but often do not provide a Phantom Line Signal. In this case, that portion of the RAM memory corresponding to the ROM memory must be permanently disabled. The 282 board is compatible with either "Bootstrap" or "Dedicated" ROMs.

PHANTOM LINE OPTION

Located on the right edge of the board, directly below the MEM ADD jack, is jack Jl. Placing a shunt on the "PH" position, second from the right, enables the Phantom Line Option. The rightmost position labeled "SP" for spare is provided for storing the shunt if the Phantom Line Option is not used.

DEDICATED ROM OPTIONS

Jacks J4 and J5 are used to disable the portion of the memory board which conflicts with DEDICATED ROMS. The user may disable from 1 to 15K bytes of memory in 1K increments starting from either end of the memory addressing or you may-disable a 1K block of memory anywhere within the memory.

Jack J4 has four positions, labeled 8, 4, 2, 1. These positions are used to select either the amount of memory to be disabled or the location of a 1K block within the memory depending upon the jack J5 shunt position.

Jack J5 has four positions, labeled 0, 1, 2, and SP. The first three are used to select whether disabling is to be done from the top (high addresses), the

DEDICATED ROM OPTIONS (Continued)

center (1K block), or the bottom (low addresses), respectively. The SP position is a spare position for shunt storage.

As shipped, the board is configured to use' all of memory with nothing disabled. The followinq table shows how to position the shunts to disable any portion of memory.

DISABLED ADDRESS TABLE

J4					J5	J5	J5
8	4	2	1	(HEX)	Shunt on "0"	Shunt on "1"	Shunt on "2"
X	X	X	X	F	0400 - 3FFF	0000 - 03FF	None
X	X	X	0	E	0800 - 3FFF	0400 - 07FF	0000 - 03FF
X	X	0	X	D	0C00 - 3FFF	0800 - 0BFF	0000 - 07FF
X	X	0	0	C	1000 - 3FFF	0C00 - 0FFF	0000 - 0BFF
X	0	X	X	B	1400 - 3FFF	1000 - 13FF	0000 - 0FFF
X	0	X	0	A	1800 - 3FFF	1400 - 17FF	0000 - 13FF
X	0	0	X	9	1C00 - 3FFF	1800 - 1BFF	0000 - 17FF
X	0	0	0	8	2000 - 3FFF	1C00 - 1FFF	0000 - 1BFF
0	X	X	X	7	2400 - 3FFF	2000 - 23FF	0000 - 1FFF
0	X	X	0	6	2800 - 3FFF	2400 - 27FF	0000 - 23FF
0	X	0	X	5	2C00 - 3FFF	2800 - 2BFF	0000 - 27FF
0	X	0	0	4	3000 - 3FFF	2C00 - 2FFF	0000 - 2BFF
0	0	X	X	3	3400 - 3FFF	3000 - 33FF	0000 - 2FFF
0	0	X	0	2	3800 - 3FFF	3400 - 37FF	0000 - 33FF
0	0	0	X	1	3C00 - 3FFF	3800 - 3BFF	0000 - 37FF
0	0	0	0	0	None	3C00 - 3FFF	0000 - 3BFF

X = Shunt On 0 = Shunt Off

Addresses shown are for the first 16K portion of RAM. For the second 16K portion, add hex '4000' to addresses, for the third 16K portion add hex '8000', and for the fourth 16K portion add hex 'C000' to addresses.

MEMORY MANAGEMENT OPTIONS

Memory Management provides a powerful tool, to expand the working RAM memory to greater than 64K bytes. Theoretically, the memory may be expanded to 4096K bytes (i.e. 4,194,304 bytes, large enough?). Memory management can be used on systems of less than 64K. Fundamentally, this system provides a means of having more than one memory with the same addressing.

Each memory board may be mapped "ON" or "OFF" via an output command to a user selected address. Bit 0 of the output word is used to enable or disable the board. A "one" bit enables the board, a "zero" disables the board. The user may interrogate the status of the board by doing an input from the same address. Again, bit 0 of the input word indicates the status; "one" indicates enabled, zero indicates disabled.

MEMORY MANAGFJ1ENT I/O ADDRESSING

Four jacks are located along the bottom of the board. Starting from the left, they are labeled ADDR 7-6, ADDR 5-4, ADDR 3-2, and ADDR 1-0. Each of these jacks is labeled 0, 1, 2, 3 with the "0" position at the top and the "3" position at the bottom.

The I/O address is selected by placing the shunts horizontally on the jacks to make up the desired I/O address. For example, if we wanted to define I/O address 7E, this would correspond to the following:

ADDR 7-6 = 1
ADDR 5-4 = 3
ADDR 3-2 = 3
ADDR 1-0 = 2

I/O address 00 is 0000, and I/O address FF is 3333.

To disable this feature, that is, to configure the board so that no I/O address is decoded, simply remove any one shunt. When shipped, the I/O address shunt on the ADDR 1-0 jack is stored on the SP of jack J5 disabling the memory management I/O address.

MEMORY MANAGEMENT INITIALIZE OPTION

When power is first applied or after "RESET", more than one board located at the same address could be mistakenly enabled. To control this situation, the left-most two positions of the Jl jack are used to determine whether the board is initially selected "ON" or "OFF".

Placing the shunt on the leftmost position, labeled "OFF", causes the board to be initialized off. Conversely, placing the shunt on the "ON" position causes the board to be initialized on.

As shipped, the board is selected ON and must be ON unless memory management is used.

POWER ON CLEAR OPTION

The "Power On Clear" line (Pin 99 on Bus) should be "pulled up" on all systems, and is to our knowledge. In the unlikely event that a manufacturer has not provided a "Power on Clear" signal with "pull-up", a jumper should be installed across the top two pads of the J3 jack location (Note: No jack or shunt is provided. J3 is located to the left of J5).

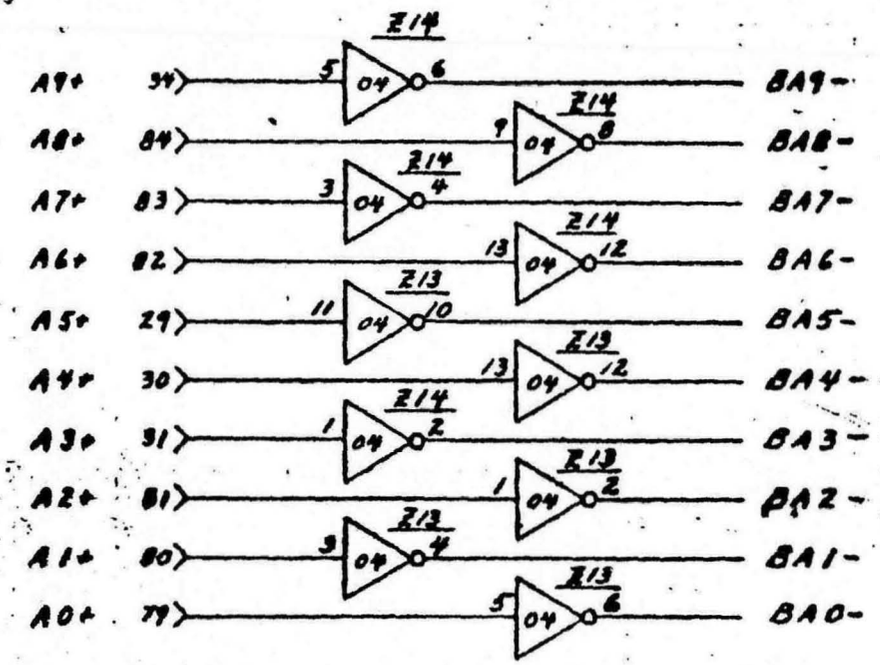
If it is desired to disable the reset signal and initialize only with "Power On Clear", the vertical trace between the leftmost two pads of J3 should be cut and the jumper installed across the top two pads.

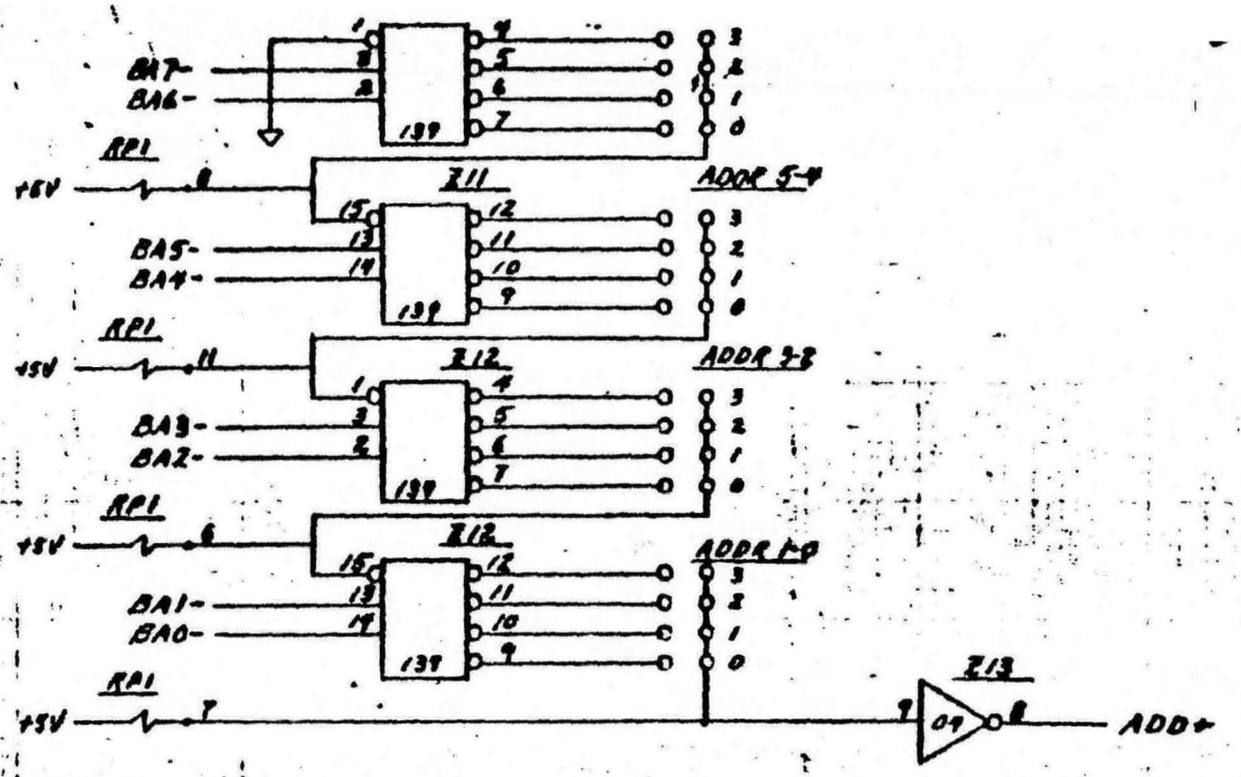
Normally, no changes are needed or desired on J3.

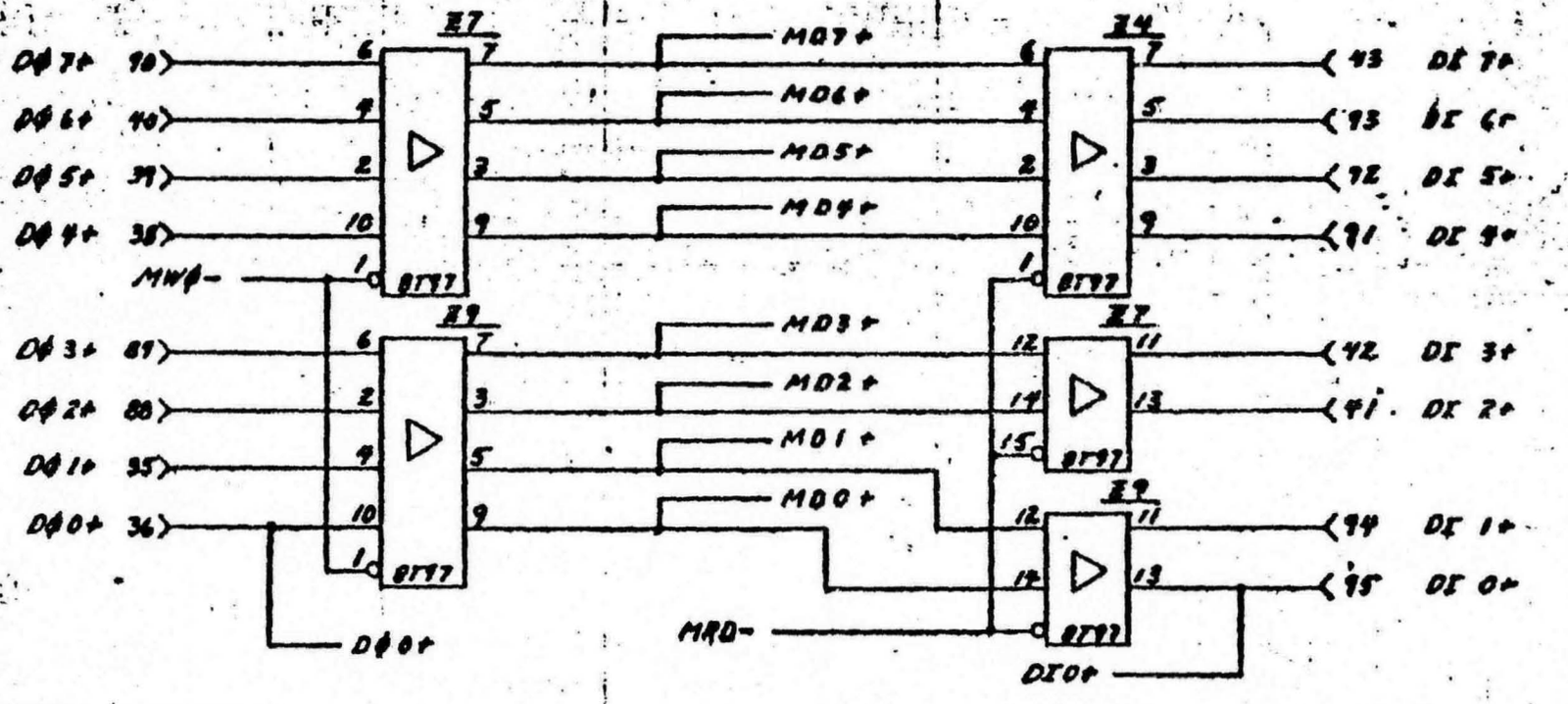
SUMMARY

Now that you have read this description we recommend strongly that all of your users read it completely before using the board and retain it for future reference. We hope that the added features of this board will provide the user with the flexibility and power he wants without undue complexity.

The 282 board has been carefully designed and uses the best of components, including a U.L. listed printed circuit board and glass encapsulated de-coupling capacitors. The board is built and tested to industrial standards and can be expected to provide long trouble free service.







MEMORY ARRAY

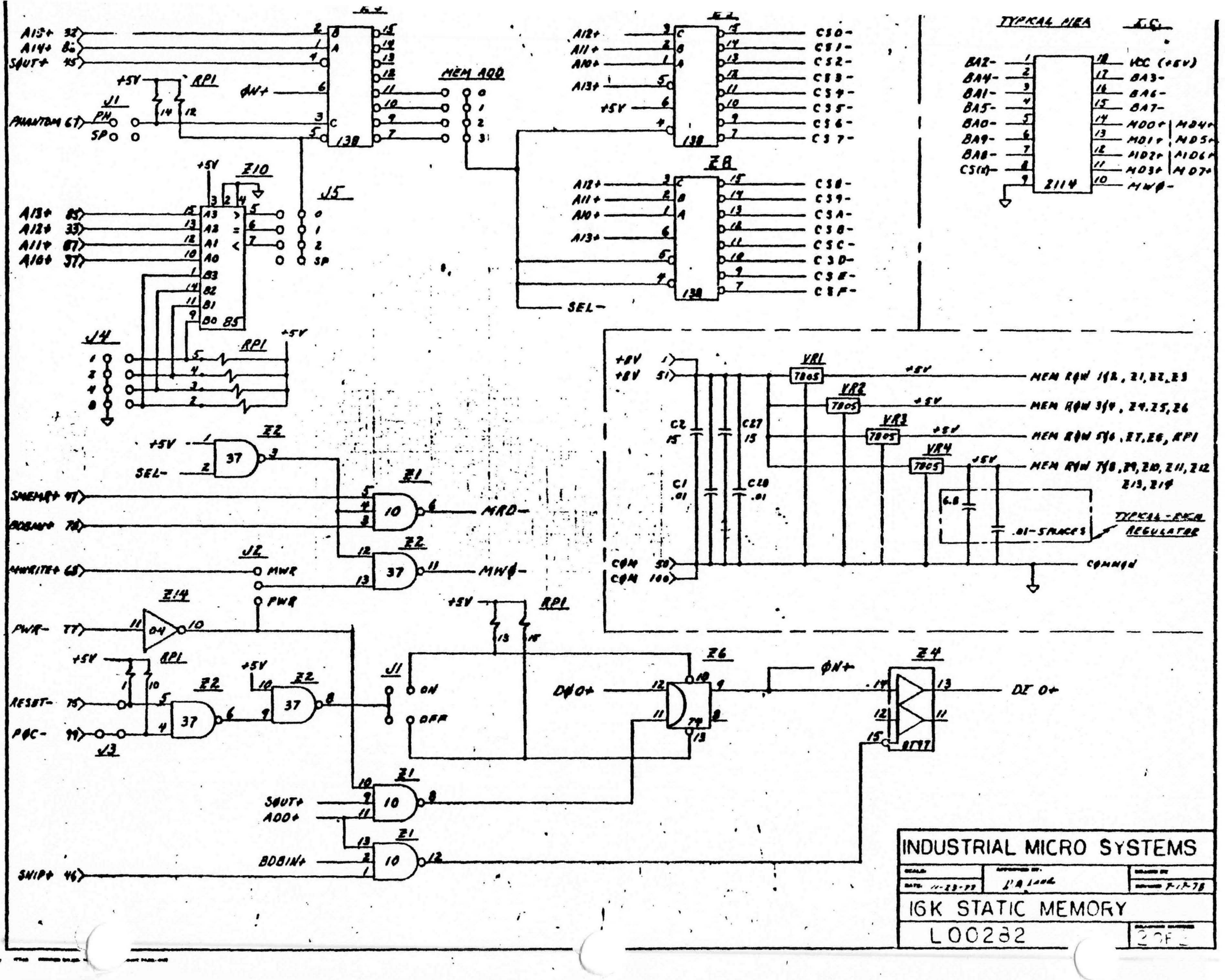
(TYP)

Row 1	CS3	CS7	CSB	CSF	MDØ-7
2	CSE	CS6	CSA	CSE	
3	CS1	CS5	CS9	CSD	
4	CS0	CS4	CS8	CSC	

5	CS0	CS4	CS8	CSC	MDØ-3
6	CS1	CS5	CS9	CSD	
7	CS2	CS6	CSA	CSE	
8	CS3	CS7	CSB	CSF	

(BOTTOM)

INDUSTRIAL MICRO SYSTEMS		
11-21-77	D.A.L.-L-	7-17-78
16K STATIC MEMORY		
L00282		1 OF 2


A13+ 32
A14+ 34
SAUT+ 45
+5V
RP1
J1
PHANTOM CT
PH
SP
14
12
ΦN+
6
3
5
138
MEM ADD
0
1
2
3
Z10
+5V
A13+ 85
A12+ 33
A11+ 87
A10+ 37
A3
A2
A1
A0
B3
B2
B1
B0
85
J15
J14
RP1
+5V
Z2
+5V
SEL-
37
SMEMR+ 41
BOBIN+ 78
Z1
10
MRD-
J2
MWR
MWRITE+ 68
Z2
37
MWΦ-
Z14
PWR
PWR- 77
04
RP1
+5V
RESET- 75
PΦC- 99
J3
Z2
37
+5V
Z2
37
J1
ON
OFF
SAUT+
ADD+
Z1
10
BOBIN+
Z1
10
SWP+ 46
+5V
RP1
13
14
Z6
DΦO+
12
11
9
8
13
ΦN+
Z4
14
12
15
13
11
DI O+
A12+
A11+
A10+
A13+
+5V
SEL-
CS0-
CS1-
CS2-
CS3-
CS4-
CS5-
CS6-
CS7-
CS8-
CS9-
CSA-
CSB-
CSC-
CSD-
CSE-
CSF-
TYPICAL MEM
BA2-
BA4-
BA1-
BA5-
BA0-
BA9-
BA8-
CS(L)-
2114
VCC (+5V)
BA3-
BA6-
BA7-
MDO+
MDI+
MD2+
MD3+
MWΦ-
MD4+
MD5+
MD6+
MD7+
+8V 1
+8V 51
VR1
7805
VR2
7805
VR3
7805
VR4
7805
+5V
MEM ROW 1/2, 21, 22, 23
MEM ROW 3/4, 24, 25, 26
MEM ROW 5/6, 27, 28, RP1
MEM ROW 7/8, 29, 210, 211, 212
213, 214
C2
.15
C27
.15
C1
.01
C28
.01
6.8
.01-SPACES
TYPICAL-EACH REGULATOR
COM 50
COM 100
COMMON
INDUSTRIAL MICRO SYSTEMS
11-23-77
P.A. Lacy
7-17-78
16K STATIC MEMORY
L00282

INDUSTRIAL

MICRO MODEL 370 32K STATIC RAM MEMORY BOARD

SYSTEMS

The 370 static RAM board is fully STATIC and fully BUFFERED using 4K X 1 memory iC's. The boards are supplied after being tested and burned in at 70° C under diagnostic test to insure reliable operations.

The 370 memory board provides 32K bytes of memory organized into 8 continuous blocks of 4K bytes each. Each 4K block may be individually turned "On" or "Off" to provide full mapping capabilities for use in systems utilizing memory management.

The 370 provides a "Phantom Line" for use in systems with ROM memories which utilize this feature. The user may also select the Processor Write (PWR) signal or the Memory Write (MWR) signal as the data strobe for storing data providing for full compatibility with "IMSAI" front panels.

The starting address of a 370 board may be located at any 4K boundary for full compatibility with systems using 4K, 8K, or 16K byte memory boards.

CONFIGURING THE 370 BOARD

starting Address

The starting address of the memory board is determined by the placement of shunts on jack J4 located in the lower right hand corner of the board. Shunts placed of J4 make up the first (most significant) HEX digit of the board's starting address. A shunt corresponds to a "one", and no shunt corresponds to a "zero". This provides for HEX starting addresses 0000, 1000, 2000,...F000.

I/O Selection

Jack J2, located in the lower right hand corner of the board, is used to select the I/O address to be used for memory mapping. The jack is labeled for the MS (most significant) and LS (least significant) halves of the I/O address. The 8 positions of J2 correspond to the 8 bits of the I/O address. A shunt corresponds to a "one"; no shunt corresponds to a "zero". Thus up to 256 unique addresses are possible.

I/O Address Enable

The left most position of jack J3, located in the lower right hand corner of the board, is used to Enable or Disable the I/O address. If memory mapping is to be used, the feature may be enabled by placing a shunt on J3. If a shunt is on J3, the 370 board will respond to the I/O address selected by the J2 shunt placements causing the memory board's addresses 1 to be mapped to the range corresponding to the starting address as determined by the shunt placements on J4.

Memory Map Control and Initializing On

The memory map register is an eight bit register that controls the "ON/OFF" state of the eight 4K blocks of the memory board. Bit 0 controls the "0" block, bit 1 the next block -

Memory Map Control and Initializing On (Continued)

* and so on. Thus for a board with a starting address selected on jack J4 of 0000, the map register bits control the address blocks as follows:

BIT	MEMORY ADDRESSES
0	0000-0FFF
1	1000-1FFF
2	2000-2FFF
3	3000-3FFF
4	4000-4FFF
5	5000-5FFF
6	6000-6FFF
7	7000-7FFF

To "RESET" or "POWER ON CLEAR" signals clear the contents of the memory map register. The exception to this occurs if a shunt is placed on the INIT position of jack Jl; in this case upon the occurrence of "RESET" or "POWER ON CLEAR", the effect is as though all 1's (hexadecimal 'FF') were output to the memory map register initializing the entire board to the "ON" state. The INIT feature simply provides a means of forcing a board Fully "ON" at system startup. If memory mapping is used and more than one board in the system is set for the same address range, it is obvious that at most one of the boards can have a shunt on the INIT position of jack Jl. After system start-up, the INIT feature is overridden by the first map command received by the board and the contents of the memory map register assume control of the "ON/OFF" states of the 4K blocks on the memory board.

PWR/MWR

This selection is made on jack Jl, located in the lower left hand portion of the board. One shunt should be placed on either PWR to select Processor Write or MWR to select Memory Write. Systems with front consoles (eg. IMSAI) should use MWR. Caution - Install only one shunt - never both PWR & MWR.

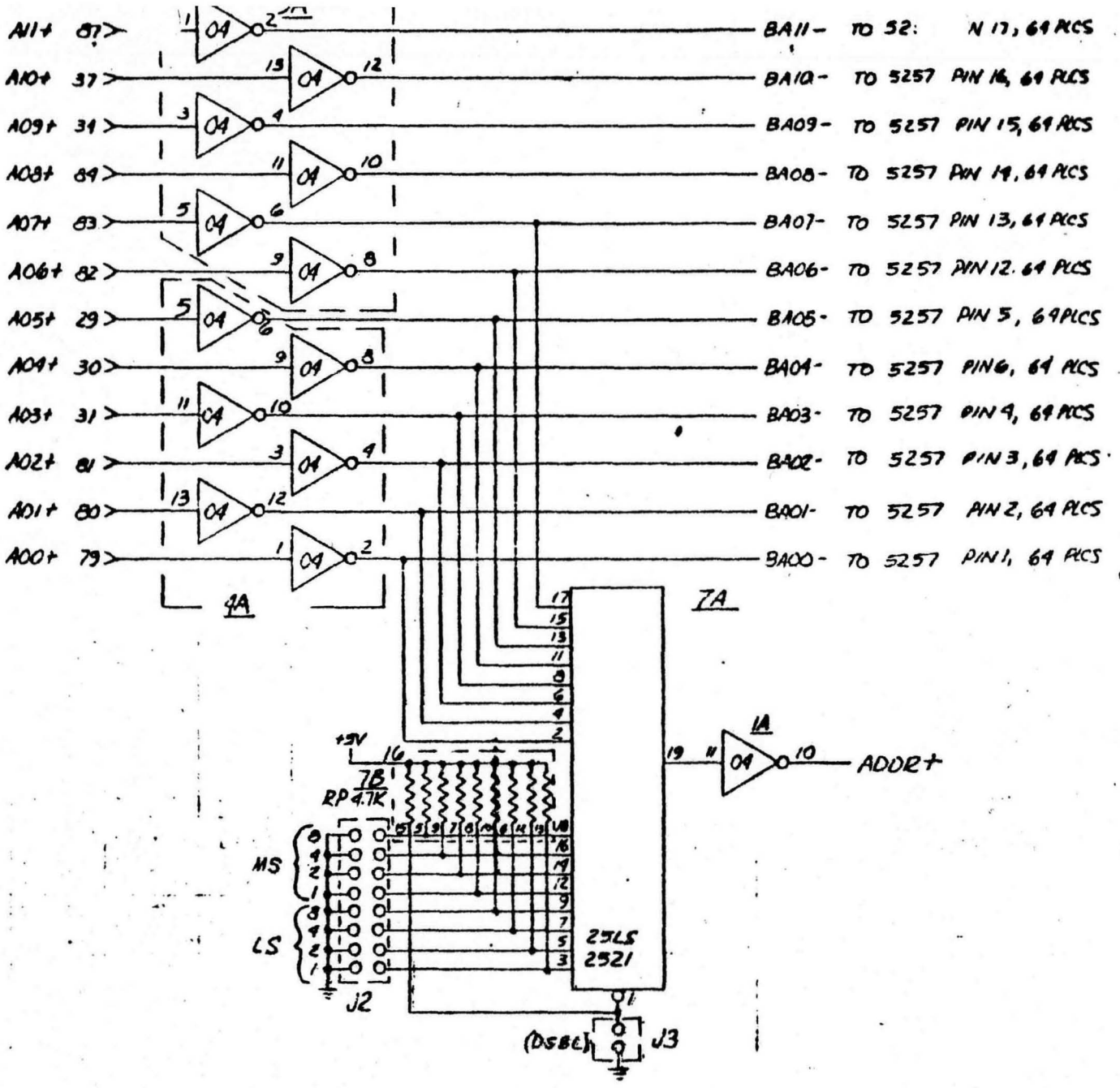
Phantom

"The Phantom Line (for systems using ROM with this feature) is enabled by placing a shunt on the PH pins on jack Jl. If this feature is not used, it is recommended that this shunt not be installed

Each of the components on this board has been selected after careful evaluation of several suppliers. Every attempt has been made to assure a high quality product manufactured to industrial standards. Pre-shipment testing and quality assurance procedures for the Industrial Micro Systems products calls for rigorous testing for shorts, opens, socket and IC problems. Subsequent to this testing the boards are subjected to dynamic "burn-in" testing at a temperature of 70° C. The gold contact material on the edge connector is lated over a nickel base to provide a high quality oxide free contact. Contact lubricants should not be used.

We strongly recommend that power be removed from a system while plugging or unplugging memory boards. Remember to allow sufficient time for the power supplies to discharge.

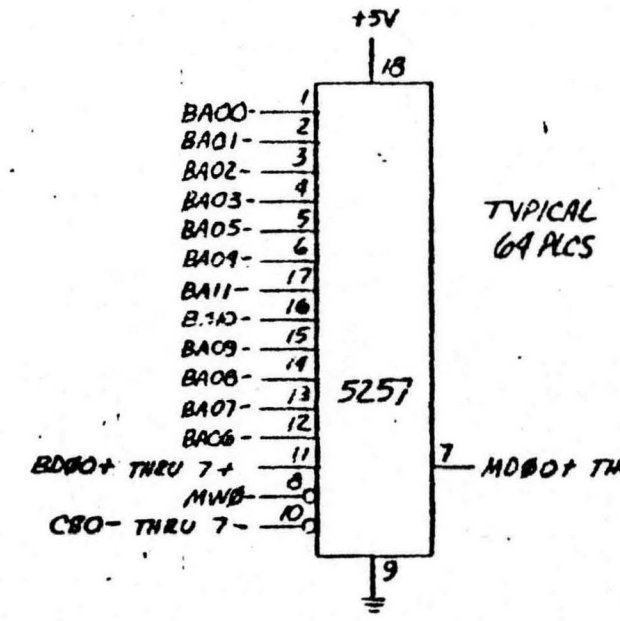
Now that you have read this description of the Industrial Micro System 370 32K byte memory board, please make certain that anyone who will be using the board does the same. Happy programming!

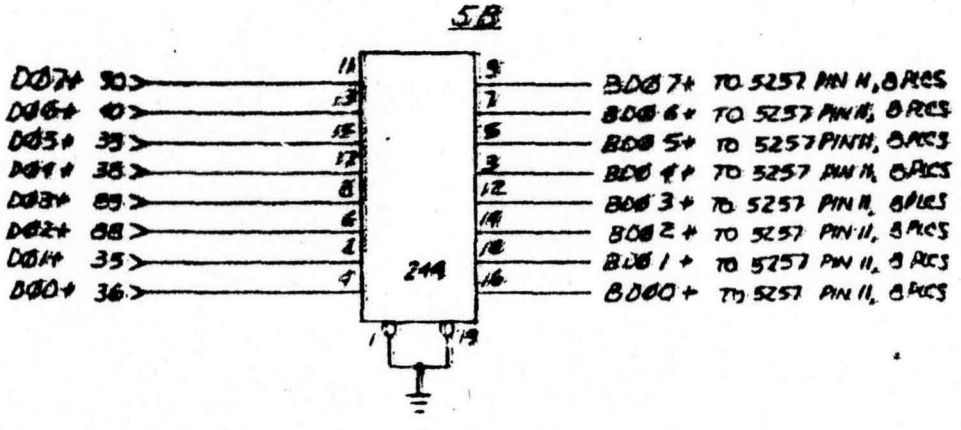


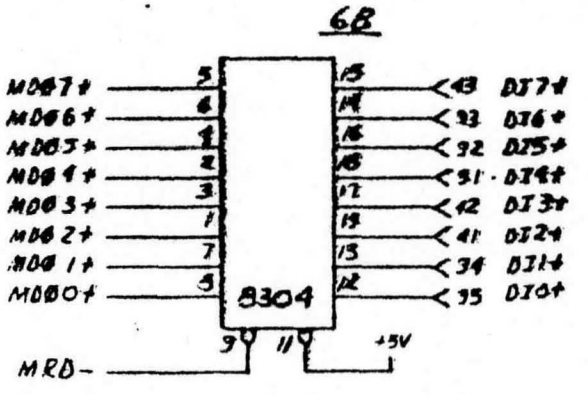
MEMORY ARRAY (5257)

	CS0	CS1	CS2	CS3	CS4	CS5	CS6	CS7
BIT7								
BIT6								
BIT5								
BIT4								
BIT3								
BIT2								
BIT1								
BIT0								

(CONNECTOR EDGE)

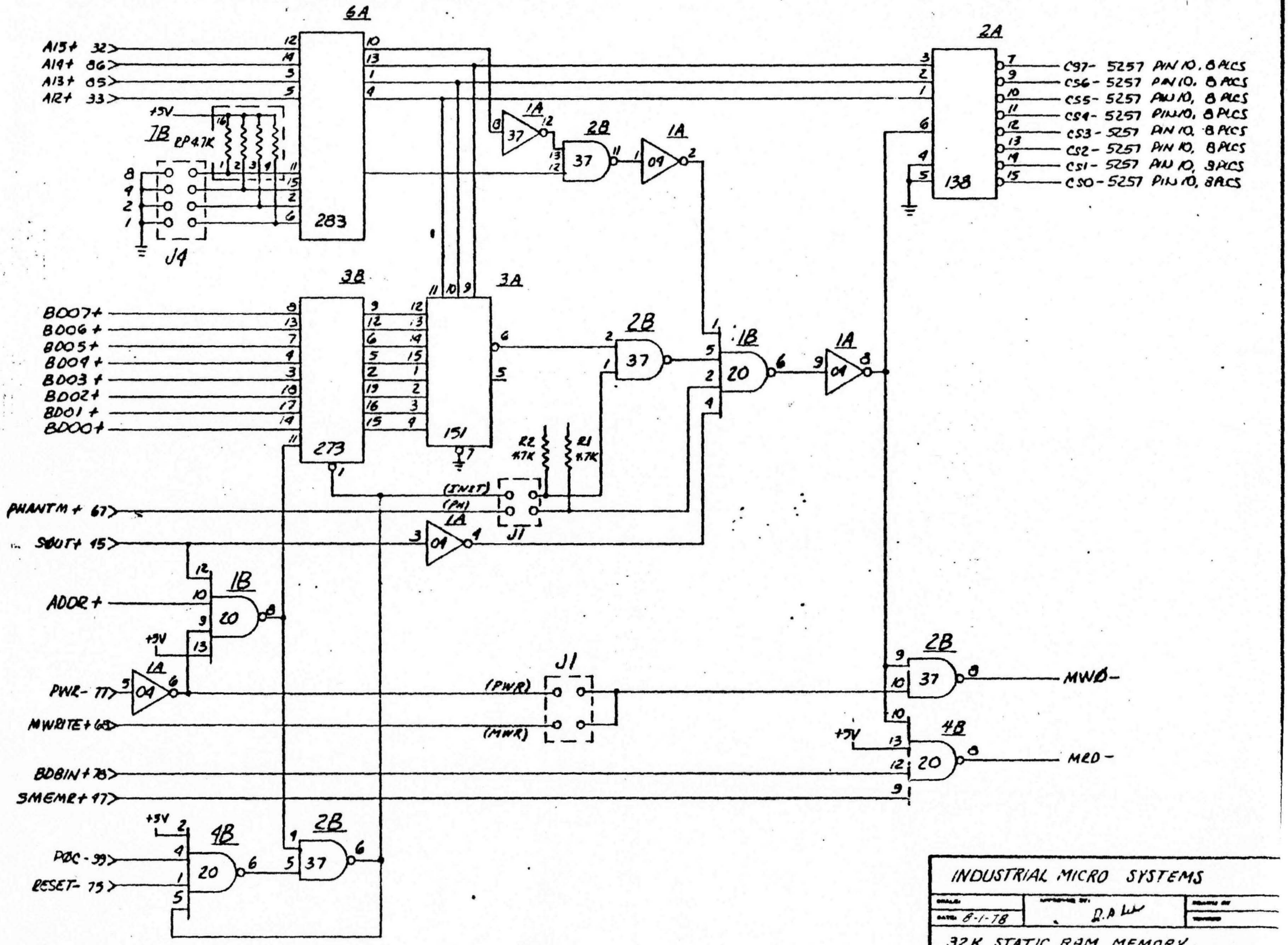




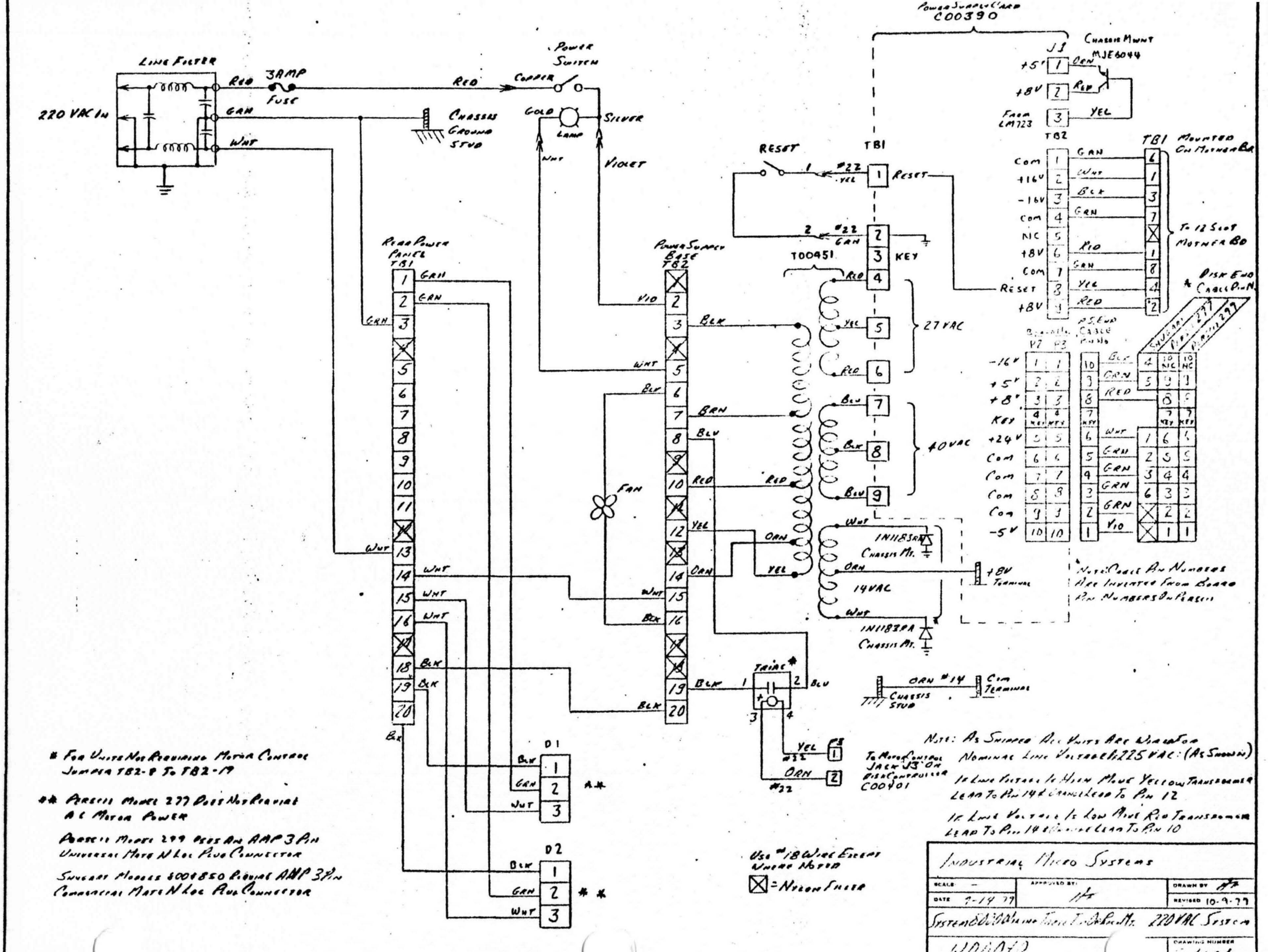


NOTE: ALL IC'S ARE 74LS EXCEPT 6B & MEMORY.

INDUSTRIAL MICRO SYSTEMS		
	D.A. LANE	
32K STATIC RAM MEMORY		
L00370		1 OF 2



INDUSTRIAL MICRO SYSTEMS		
DRAWN	APPROVED BY: D.A.W	DRAWING NO.
DATE 8-1-78		REVISED
32K STATIC RAM MEMORY		
L00370		SHEET 2 OF 2

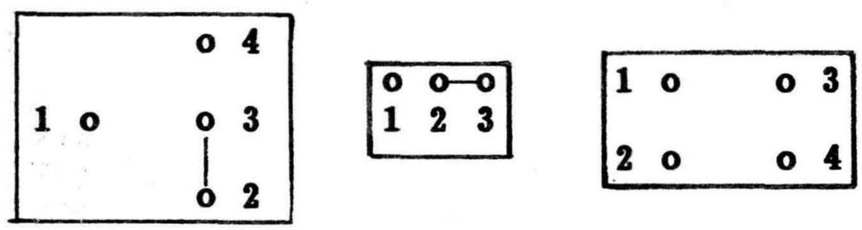


Power Supply Card
C00390
Line Filter
220 VAC In
Red
3AMP
Fuse
GRN
WHT
Chassis Ground Stud
Power Switch
Copper
Gold
Silver
Lamp
WHT
Violet
Red
Chassis Mount MJE6044
J1
+5V
+8V
ORN
Red
YEL
From LM723
TB2
TB1 Mounted On Mother Bd
To 12 Slot Mother Bd
RESET
TB1
#22 YEL
#22 GRN
Reset
KEY
T00451
27VAC
40VAC
14VAC
Com
+16V
-16V
Com
NC
+8V
Com
Reset
+8V
Rear Power Panel TB1
Power Supply Base TB2
GRN
WHT
BLK
BRN
BLU
RED
YEL
ORN
VIO
Fan
IN1183RA Chassis Mt.
+8V Terminal
Triac *
D1
D2
ORN #14
Com Terminal
Chassis Stud
Disk End * Cable Pin No.
-16V
+5V
+8V
Key
+24V
Com
-5V
Note: Cable Pin Numbers Are Inverted From Board Pin Numbers On Persci
* For Units Not Requiring Motor Control Jumper TB2-8 To TB2-19
** Persci Model 277 Does Not Require AC Motor Power
Persci Model 299 Uses An AMP 3 Pin Universal Mate N Loc Plug Connector
Shugart Models 800 & 850 Require AMP 3 Pin Commercial Mate N Loc Plug Connector
To Motor Control Jack J3 On Disk Controller C00401
Note: As Shipped All Units Are Wired For Nominal Line Voltage Of 225 VAC (As Shown)
If Line Voltage Is High Move Yellow Transformer Lead To Pin 14 & Orange Lead To Pin 12
If Line Voltage Is Low Move Red Transformer Lead To Pin 14 & Orange Lead To Pin 10
Use #18 Wire Except Where Noted
= Nylon Sheer
Industrial Micro Systems
Scale —
Date 9-14-79
Revised 10-9-79
220VAC System
W00070
Sh 1 of 1

CONFIGURING THE 440 I/O BOARD

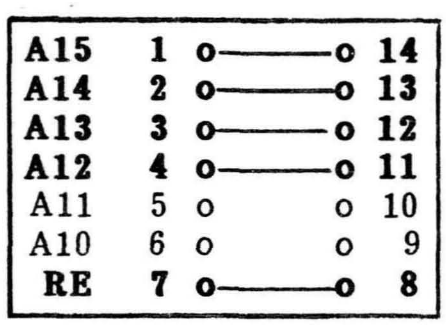
To Use a 2732 4K x 8 PROM:

JD JE JF



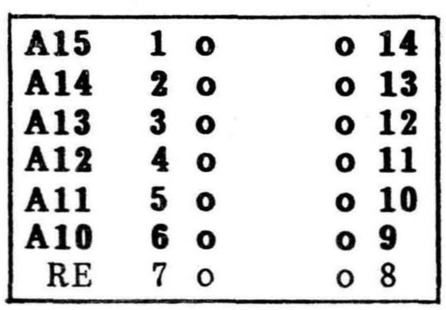
Shunt JD 2-3
Shunt JE 2-3
No shunts at JF
Remove shunts A10 and A11 at JG

JG



EPROM Address Select (Pad JG)

JG



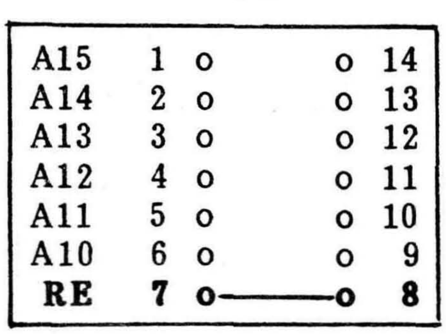
Shunt OFF = 1 Shunt ON = 0

All Shunts OFF = EPROM Starting Address X' FC00'

All Shunts ON = EPROM Starting Address X' 0000'

EPROM Enable (RE at Pad JG)

JG



Shunt OFF "RE" = EPROM Disabled

Shunt ON "RE" = EPROM Enabled

Thiel
100 180 293
KSK Clausthal/Zellerfeld
268514 10

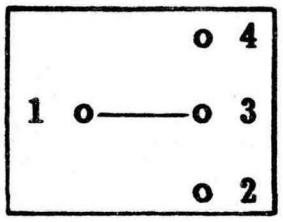
CONFIGURING THE 440 I/O BOARD

ROM SELECT (PADS JD, JE, JF, JG)

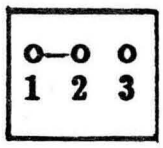
Any connections made by etch which are not defined in the following diagrams should be cut.

To Use a 2708 1K x 8 EPROM:

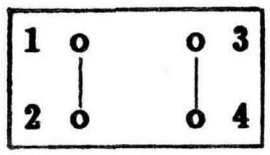
JD



JE

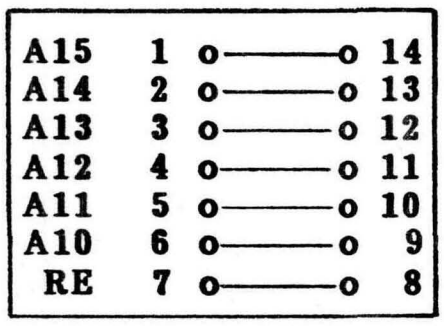


JF



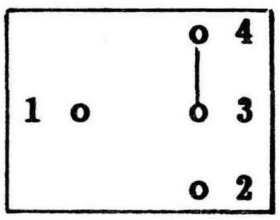
Shunt JD 1-3
Shunt JE 1-2
Shunt JF 1-2
Shunt JF 3-4
Shunt all horizontally at JG

JG

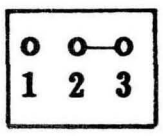


To Use a 2716 2K x 8 EPROM:

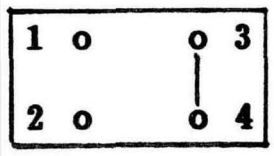
JD



JE



JF



Shunt JD 3-4
Shunt JE 2-3
Shunt JF 3-4
Remove shunt A10 at JG

JG